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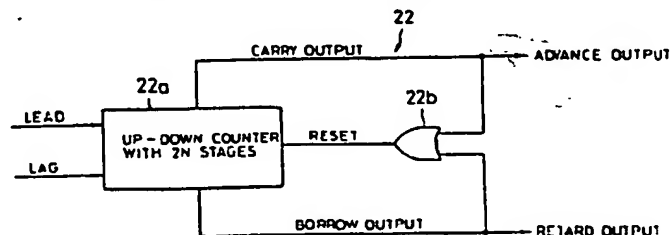
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54 Digital phase-locked loops.

57 A digital phase-locked loop in which the lead or lag of the phase of the input is compared to the phase of the output of the loop and the occurrences of the advance or retardation are filtered in a random walk filter in order to phase control the output. According to the invention, the time trend of the advance or retardation is determined. If there is a significant run of either advance or retardation, the random walk filter is adjusted so as to more quickly provide correcting output.

FIG. 2 PRIOR ART



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## DIGITAL PHASE-LOCKED LOOPS

BACKGROUND OF THE INVENTIONField of the Invention

The present invention relates to a digital phase-locked loops. It particularly relates to a digital phase-locked loop in which a random walk filter is used to effectively suppress the jitter of an input signal.

Background of the Invention

A conventional digital phase-locked loop has been used for many purposes such as signal retiming and signal selection (refer to "IEEE Transactions on Communications", vol. COM-20, No. 2, page 95, April, 1972: Title: Phase Noise and Transient times for a Binary Quantized Digital Phase-Locked Loop in White Gaussian Noise, written by JAMES R. CESSNA, DONALD M. LEVY). In the conventional digital phase-locked loop shown in Figs. 1, an input digital signal to the system and the output signal of a scaler 25 are supplied to a binary phase detector 21. These Selective output of the binary phase detector 21 is a lead output or a lag output and is selectively supplied to a random walk filter 22. An advance input or a retard input is sent from the random walk filter 22 to a phase controller 24. An oscillator 23 supplies to the phase controller 24, whose frequency is much higher than that of

the input digital signal. The output of the phase controller 24 is frequency-divided by the scaler 25, the output of which is sent to the outside of the digital phase-locked loop as well as fed back to the binary phase detector 21.

As shown in Fig. 2, the major part of the random walk filter 22 is an up-down counter 22a having  $2N$  stages. The count of the counter 22a is increased by one every time the lead input is supplied thereto. The count of the counter 22a is decreased by one every time the lag input is supplied thereto. The carry output of the up-down counter 22a is used as the advance output. The borrow output of the counter 22a is used as the retard output. The output signal of an OR gate 22b, which receives both the outputs, is supplied to the resetting terminal of the up-down counter 22a to reset the count of the counter to  $N$ .

When the lead input has been supplied a number of times which is  $N$  more than that of the supply of the lag input the advance output is sent out from the up-down counter 22a for the phase controller 24 to delay the phase of the output of the stable fixed oscillator 23. Thereafter, the scaler 25 frequency divides the phase delayed signal to send out a signal compensated for the phase deviation.

When the lag input has been supplied a number of times  $N$  more than that for which the lead input has been supplied, the retard output is sent out from the up-down counter 22a to advance the phase of the output of the stable fixed oscillator 23 by the phase controller 24. The phase advanced output is frequency divided by the scaler 25 to send out a signal compensated for the phase deviation.

As understood from the above description, the control of the phase is not necessarily performed immediately after the supply of the lead input or the lag input but is performed only when the number of times of the supply of one of the lead input and the lag input has become  $N$  more than that of times of the supply of the other. As a result, the jitter of the input digital signal can be suppressed to stabilize the phase of the output signal.

In the above-described conventional digital phase-locked loop, the effect of the jitter suppression can be enhanced by increasing the number of the stages of the up-down counter 22a. However, if the number of the stages of the up-down counter 22a is increased, the response time of the digital phase-locked loop is lengthened in proportion to the increased number of the stages so that the effect of the jitter suppression and the transient characteristic

of the loop conflict with each other. In other words, the transient characteristic is degraded if the effect of the jitter suppression is enhanced and the effect of the jitter suppression is degraded if the transient characteristic is enhanced.

#### SUMMARY OF THE INVENTION

The present invention was made in consideration of the above-described problem.

Accordingly it is an object of the present invention to provide a digital phase-locked loop whose jitter suppression effect and transient characteristic are both enhanced.

The digital phase-locked loop provided in accordance with the present invention includes a phase deviation trend detection means which receives an lead input and a lag input and sends out a phase deviation trend indication output. A reference value control means receives the phase deviation trend indication pulses from the phase deviation trend detection means and alters a reference value for a random walk filter depending on the trend of phase deviation.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 show circuit diagrams of a conventional digital phase-locked loop.

Fig. 3 shows a circuit diagram indication the electrical design of a digital phase-locked loop provided in accordance with the present invention.

Fig. 4 shows a circuit diagram indicating the electrical design of the major part of the digital phase-locked loop.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the digital phase-locked loop provided in accordance with the present invention, the phase of an input signal is determined to supply either the lead input or the lag input. The lead or lag input is supplied to the random walk filter which supplies a phase advance control pulses or a phase delay control pulses to a phase controller which outputs a signal compensated for the phase deviation. At that time, the trend of the phase deviation is determined by the phase deviation trend detection means in terms of the lead input or the lag input so that the reference value supplied to the random walk filter is altered depending on the trend of the phase deviation. The reference value control means alters the reference value in terms of the phase deviation trend indication pulses sent out from the phase deviation trend detection means.

Since the phase deviation usually occurs in such a manner that the phase is only lead or only lag, a

sufficient effect of jitter suppression can be produced even if the reference value for the random walk filter is altered in a unidirectional manner at the time of the detection of the phase deviation so as to control the phase by a reduced number of times of supply of the input indication pulses.

An embodiment of the present invention is hereafter described in detail with reference to the drawings attached hereto.

Fig. 3 shows a circuit diagram of a digital phase-locked loop which is an embodiment of the invention. The loop comprises a binary phase detector 1, a random walk filter 2, a fixed stable oscillator 3, a phase controller 4, a scaler 5, a phase deviation trend detector 6 and a reference value controller 7.

The binary phase detector 1 receives an input digital signal to the system and a frequency-divided signal from the scaler 5 and judges whether the phase of the input digital signal is advanced or retarded. The detector 1 then sends out an lead input or a lag input

The random walk filter 2 is made of a up-down counter having  $2N$  stages. The count of the counter is increased by one every time the lead input is supplied thereto. The count of the counter is decreased by one every time the lag input is supplied thereto. The filter

2 sends out a carry pulse as an advance output or a borrow pulse as a retard output.

The fixed stable oscillator 3 sends out a signal whose frequency is much higher than that of the input digital signal (for instance, the frequency of the signal of the oscillator 3 is 1.6 MHz when that of the input digital signal is 100 kHz).

The phase controller 4 regulates the frequency of the signal of the fixed oscillator 3 depending on the advance output or the retard output.

The scaler 5 frequency-divides the output signal of the phase controller 4 to a frequency of a value  $1/k$  of the input frequency ( $k$  denotes a preset integer; the greater the integer is made, the smaller the phase deviation in a stationary state is made).

Fig. 4 shows a detailed circuit diagram of the random walk filter 2, the phase deviation trend detector 6 and the reference value controller 7.

The lead input is supplied to the up-counting input terminal of the random walk filter 2, while the retarded input is supplied to the down-counting input terminal of the filter. When a load pulse of the reference value controller 7 is supplied to the load terminal of the filter 2, a numerical value signal of the controller 7 is supplied to the presetting input terminals

of the filter 2. The filter 2 sends out the carry pulses as the advance output or the borrow pulses as the retard output, similarly to the up-down counter 22a of Fig. 2.

The major part of the phase deviation trend detector 6 is a shift register 8 having  $m$  stages. The output of an OR gate 9, which receives the lead input and the lag input is supplied as a lock signal to the shift register 8. The lead input is supplied as a data pulses to the shift register 8. The parallel output of all the stages of the shift register 8 are supplied to a first AND gate 10 without being inverted. Additionally, the output signals of all the stages of the shift register 8 are inverted and then supplied to a second AND gate 11. The output of the first and the second AND gates 10 and 11 are supplied to AND gates 12 and 13, which are opened by the output of the OR gate 9 receiving the lead and retard input indication signals. The output of the AND gates 10 and 11 are inverted and then supplied to a NAND gate 14. The number  $m$  is determined depending on the number  $2n$  of the stages or counting range of an up-down counter 15 described hereinafter. It is preferable to determined the number  $m$  to most enhance both the jitter suppression and the response of the digital phase-locked loop.

The reference value controller 7 comprises the up-down counter 15 and an OR gate 16. The output signal of

the AND gate 12 is supplied as an advance reference value control signal to the up-counting input terminal of the up-down counter 15. The output signal of the AND gate 13 is supplied as a retard reference value control signal to the down-counting input terminal of the up-down counter 15. The output of the NAND gate 14 is supplied to the resetting input terminal of the up-down counter 15.

The output of the OR gate 16, which receives the advance output and the retard output, is supplied to the load terminal of the random walk filter 2. The numerical value output of the up-down counter 15 is supplied to the presetting input terminal of the random walk filter 2.

Since the operation of the digital phase-locked loop of the above-described constitution is nearly the same as that of a conventional digital phase-locked loop, only the operation of the loop part shown in Fig. 4 is hereafter described.

When the lead input is supplied (a high-level signal is output), the contents of the shift register 8 are sequentially shifted to the right and the content of the first stages thereof is set at a high level.

When the lag input is supplied as a high level signal, the contents of the shift register 8 are sequentially shifted to the right and the content of the first step thereof is set at a low level.

When only the lead input is supplied  $m$  sequential and uninterrupted times, the contents of all the stages of the shift register 8 are set at a high level so that the first AND gate 10 sends out a high-level signal. The high-level signal is supplied to the up-counting input terminal of the up-down counter 15 through an AND gate 12 opened at the timing of the rising of the output signal of the OR gate 9, so that the count of the up-down counter 15 is increased by one.

When only the lag input is supplied  $m$  sequential and uninterrupted times, the count of the up-down counter 15 is similarly decreased by one.

When neither of the lead input and the retard input is individually supplied  $m$  sequential times, the output signals of the AND gates 10 and 11 both remain at a low level so that the NAND gate 14 sends out a high-level signal to reset the count of the up-down counter 51 to an intermediate value  $n$ .

Since the lead input and the lag input are being continuously supplied to the random walk filter 2 during the above-described operation, it is filled with a content corresponding to the difference between the number of times of the supply of the lead input and number of times for the lag input. When the difference has reached a prescribed number, the carry pulses or the borrow signal

is sent out. The phase controller 4 can be regulated depending on the carry pulses or the borrow pulses.

When the carry pulses or the borrow pulses is sent out, the OR gate 16 supplies the load pulses to the random walk filter 2 so that an initial value is preset by the present count of the up-down counter 15.

For these reasons, when the lead input is supplied  $m$  sequential times, for instance, the count of the up-down counter 15 becomes  $n+1$  so that the carry output is sent out when the number of times of the supply of the lead input is less by one than in the conventional random walk filter. After that, the count of the up-down counter 15 is increased every time yet another lead input is supplied to the random walk filter 2. When the carry pulses is sent out from the random walk filter 2 the next time, the increased count of the up-down counter 15 is the value which is preset into the random walk filter 2. For that reason, the carry pulses can be sent out from the random walk filter after a reduced number of times of the supply of the lead input

Since the count of the up-down counter 15 is decreased when the lag input is continuously supplied  $m$  or more times, the number of times of input of the lag input which is necessary to send out the borrow pulses, can be reduced.

When the lag input is supplied to the random walk filter 2 during the continuous supply of the lead input thereto or vice versa, the output signals of the AND gates 10 and 11 are both immediately set at a low level so that the NAND gate 14 sends out a high-level signal to reset the count of the up-down counter 15 to the intermediate value.

Since the AND gates 12 and 13 are opened at the timing of the rising of the output signal of the OR gate 9, the accuracy of the operation is enhanced.

The above description is hereafter summarized. When the trend of the lead or lag of the phase is continuing, the count of the up-down counter 15 is increased or decreased and the present value of the random walk filter 2 is reset to the count of the up-down counter 15 at prescribed timing. For that reason, the number of times of the supply of the input indication signal, which is necessary to be performed until the carry signal or the borrow signal is sent out, is reduced to quicken the response of the filter 2. When the trend of the advance or delay of the phase has stopped continuing, the count of the up-down counter 15 is reset to the intermediate value. For that reason, the jitter suppression effect of the filter 2 is enhanced.

The present invention is not confined to the above-described embodiment, but may be embodied in other various ways without departing from the spirit or essential character of the inventions. For instance, the phase deviation trend detector may be made of a microcomputer if very rapid filtering does not need to be performed.

CLAIMS

What is claimed is:

1. A digital phase-locked loop circuit, comprising:

means for determining a phase of an input signal relative to an output signal to selectively supply one of an lead input and a lag input;

a random walk filter receiving said lead and lag input to thereby supply one of a phase advance output and a phase retard output;

phase control means receiving said phase advance and retard outputs for providing a phase compensated signal being said output signal;

phase deviation trend detection means receiving said advanced and delayed input indications signal for detecting a trend of a deviation of said phase to thereby produce a phase trend indication signal; and

a reference value control means for altering a reference value supplied to said random walk filter responsive to said phase trend indication signal.

2. A digital phase-locked loop circuit as recited in Claim 1, wherein said phase deviation trend detection means comprises:

means for detecting at least one predetermined sequence of said lead and lag input indications signals.

3. A digital phase-locked loop circuit as recited in Claim 2, wherein said sequence detecting means comprises:

- a clock synchronized with said lead and lag input;
- a shift register clocked by said clock and receiving one of said lead and lag input; and
- two linear logic circuits receiving a first combination and a second combination inverted from said first combination of parallel outputs of said shift register.

4. A digital phase-locked loop circuit as recited in Claim 1, wherein said reference value control means comprises an up down counter counted by and resettable by signals from said phase deviation trend detection means.

5. A digital phase-locked loop circuit as recited in Claim 4, wherein said reference value control means further comprises logic means responsive to said advance and retard control signals for presetting an initial value of said random walk filter with an output of said up down counter.

6. A digital phase-locked loop circuit as recited in Claim 5, wherein said sequence detecting means comprises:

- a clock synchronized with said lead and lag input;

a shift register clocked by said clock and receiving one of said lead and lag input;

two linear logic circuits receiving a first combination and a second combination inverted from said first combination of parallel outputs of said shift register;

gating circuits controlled by said clock connected between said two linear logic circuits and counting inputs of said up down counter; and

a logic circuit connected between said two linear logic circuits and a resetting input of said up down counter.

7. A method of synchronizing a phase loop, comprising the steps of:

determining a phase of an input signal relative to an output signal;

selecting a lead input or a lag input responsive to said determining step;

determining occurrences of said lead input and said lag input relative to each other and to a reference value to thereby select a phase advance condition or a phase retard condition;

providing a phase compensated signal related to said input signal responsive to said selected phase

advance and retard conditions, said phase compensated  
signal being said output signal;

detecting a trend of a deviation of said phase;  
and

varying said-reference value in response to said  
detected trend.

Neu eingereicht / Newly filed  
Nouvellement déposé

FIG. 1 PRIOR ART

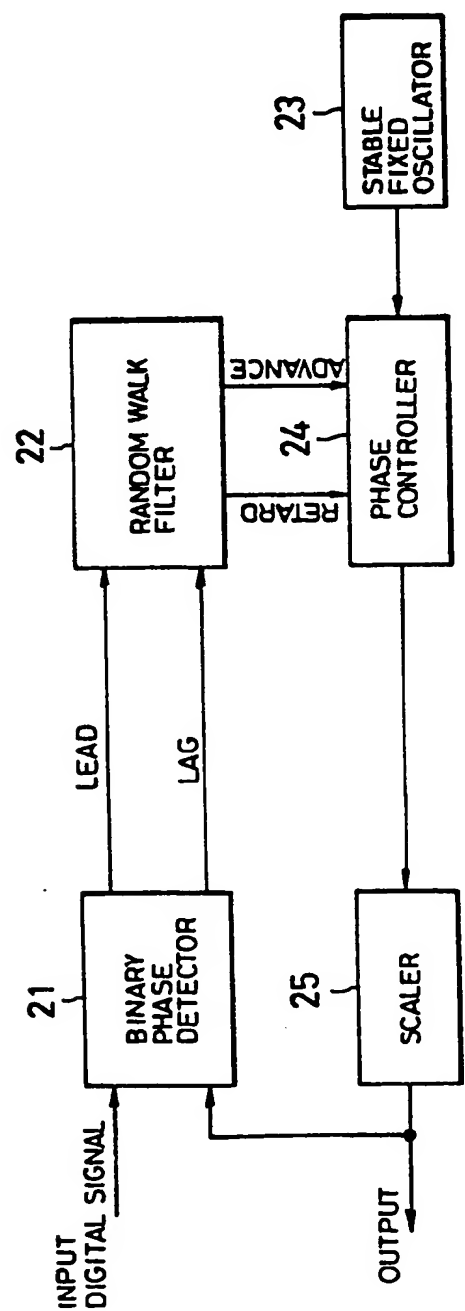


FIG. 2 PRIOR ART

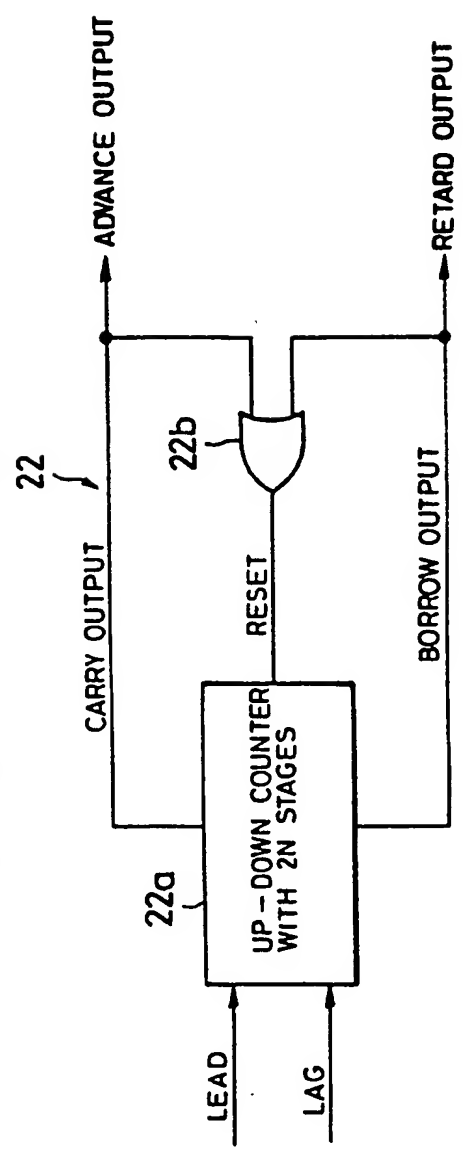


FIG. 3

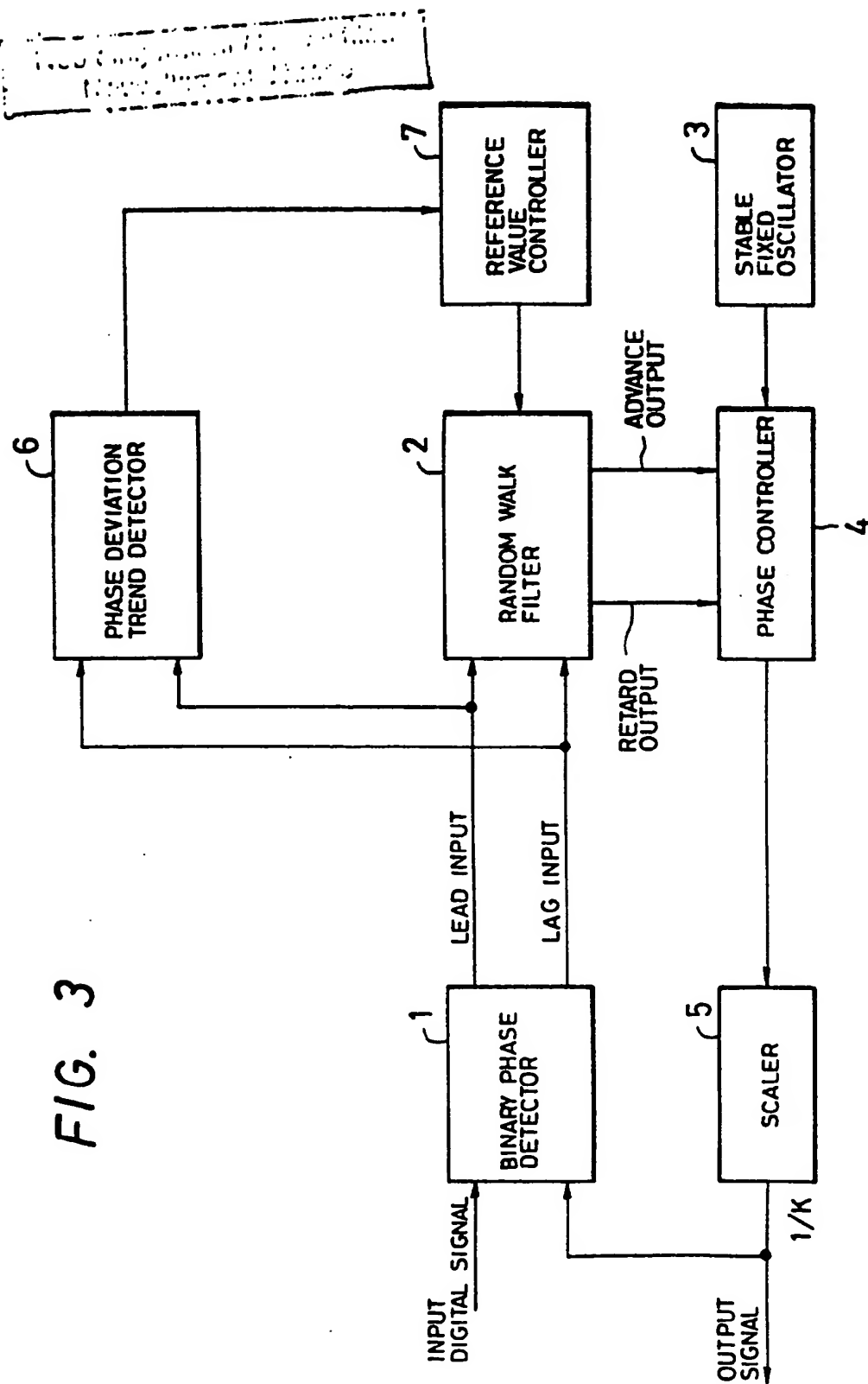
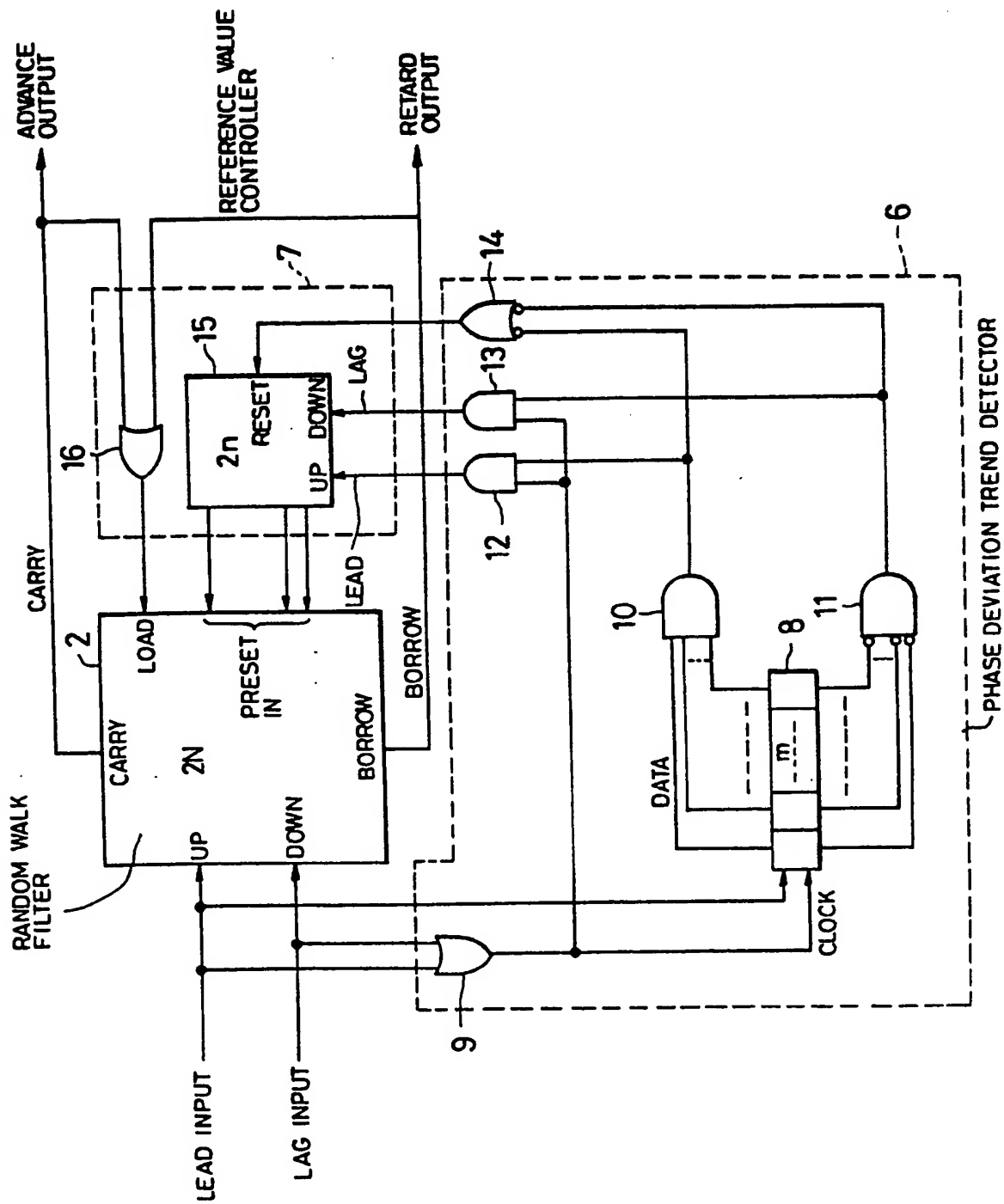


FIG. 4



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Date of publication of application: **13.01.88**  
Bulletin 88/2

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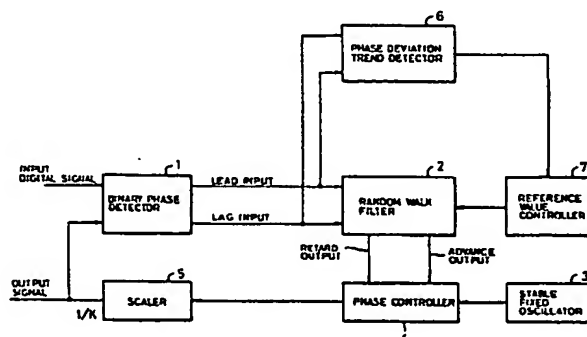
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**Digital phase-locked loops.**

In a phase detector (1) the lead or lag of the phase of the input signal is compared to the phase of the output signal of the loop. The output of the phase detector is filtered by a random walk filter (2) and applied to a phase controller (4) in order to control the output phase of a fixed oscillator (3). A phase deviation trend detector (6) determines the trend of the phase difference and if there is a significant deviation of the phase the random walk filter is adjusted so as to provide for a more rapid phase correction of the output.



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# EUROPEAN SEARCH REPORT

0252444

Application Number

EP 87 10 9554

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
X	IEEE TRANSACTIONS ON COMMUNICATIONS, vol. COM-26, no. 1, January 1978, pages 35-45, IEEE, New York, US; H. YAMAMOTO et al.: "Performance of a binary quantized all digital phase-locked loop with a new class of sequential filter" * Page 35, left-hand column, line 1 - page 36, right-hand column, line 18; figures 1,2,3 *	1,2,4,5 ,7	H 03 L 7/00 H 04 L 7/02
Y	IDEM ---	3,6	
X	ELECTRONICS & COMMUNICATIONS IN JAPAN, vol. 63; no. 12, December 1980, pages 65-72, 1982 Scripta Publishing Co., Silver Spring, Maryland, US; S. SUZUKI et al.: "High-speed digital PLL using trigger oscillators" * Page 68, right-hand column, line 11 - page 71, left-hand column, line 19; figures 10,12 *	1,2,4,5 ,7	
Y	IDEM ---	3,6	
Y	ELECTRONICS & COMMUNICATIONS IN JAPAN, vol. 63, no. 5, May 1980, pages 29-37, 1982 Scripta Publishing Co., Silver Spring, Maryland, US; T. KURITA et al.: "A digital phase-locked loop with AND filter" * Page 29, right-hand column, line 33 - page 30, right-hand column, line 27; figures 1-3 * --- -/-	3,6	H 03 L H 04 L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18-07-1988	Examiner DHONDT I.E.E.
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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# EUROPEAN SEARCH REPORT

0252444

Application Number

EP 87 10 9554

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
D,A	IEEE TRANSACTIONS ON COMMUNICATIONS, vol. COM-20, no. 2, April 1972, pages 94-104; J.R. CESSNA et al.: "Phase noise and transient times for a binary quantized digital phase-locked loop in white Gaussian noise" * Figures 1,11 * -----	1,7	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 18-07-1988	Examiner DHONDT I.E.E.
<b>CATEGORY OF CITED DOCUMENTS</b> X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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